I claim:

SUB B1

1. A computer-implemented method for remapping between pixel coordinate space and memory address space, comprising the steps of:

a) defining a phantom port containing a plurality of memory addresses;

b) generating an address to the phantom port using a conventional addressing scheme;

c) determining an address in memory address space corresponding to the generated phantom port address; and

d) accessing the address in memory address space.

2. The method of claim 1, wherein b) comprises generating an address to the phantom port using a linear addressing scheme.

3. The method of claim 1, wherein b) comprises generating an address to the phantom port using a tiled addressing scheme.

4. The method of claim 1, wherein the phantom port has a span size equal to a power of two.

5. The method of claim 4, wherein c) comprises determining an address in memory address space by extracting at least one field from the phantom port address.

6. A computer-implemented method for accessing representations of pixels for a display panel in a frame buffer, each pixel having a first coordinate and a second coordinate, the method comprising the steps of:

a) determining a span of first coordinates of pixels of the display panel;

b) defining a virtual frame buffer having a first dimension at least as large

as the span of the first coordinates;

c) generating a virtual address indicating a first coordinate and second coordinate of a pixel from the first dimension of the virtual frame buffer and the first and second coordinates of the pixel, with the virtual address identifying a memory cell; and

d) performing one of a reading operation and a writing operation of a representation of the pixel in the memory cell identified by the virtual address.

Sub a2

7. The method of claim 6, further comprising:

f) repeating b) through d) for each of a plurality of pixels having first coordinates in the determined span.

8. The method of claim 6, further comprising:

f) defining a base value, and wherein the first dimension of the virtual frame buffer is a power of the base value.

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~~9.~~ The method of claim ~~8~~, wherein the first and second coordinates of the pixel are stored as bit representations and the base value is defined as a power of two.

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5 ~~10.~~ The method of claim ~~6~~, wherein the first and second coordinates of the pixel are stored as bit representations and c) comprises concatenating the bit representation of the first coordinate of the pixel to the bit representation of the second coordinate of the pixel.

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~~11.~~ The method of claim ~~6~~, wherein d) comprises converting the generated virtual address into a memory address in a memory address range of the frame buffer and performing one of a reading operation and a writing operation of a repre-

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sentation of the pixel in a memory cell identified by the memory address.

7 ~~12.~~ The method of claim ~~6,~~ 1 wherein d) comprises performing one of a reading operation and a writing operation of a representation of the pixel in a memory cell identified by the virtual address in a frame buffer addressed by the addresses of the virtual frame buffer.

8 ~~13.~~ The method of claim ~~12,~~ 7 wherein the frame buffer is addressed by the addresses of the virtual frame buffer that represent virtual addresses of pixels of the display panel.

9 ~~14.~~ A computer-implemented method for accessing representations of pixels of a display panel in a frame buffer, the display panel having a plurality of pixels each pixel having a first coordinate and a second coordinate, the method comprising the steps of:

a) determining a span of first coordinates of pixels of the display panel;

b) selecting a second tile span representing a length of a tile of the display panel along the second coordinates of pixels of the display panel;

c) defining a virtual frame buffer having a first dimension at least as large as the span of the first coordinates times the second tile span;

d) generating a virtual address indicating a first coordinate and a second coordinate for a pixel from the first dimension of the virtual frame buffer and the first and second coordinates of the pixel; and

e) performing one of a reading operation and a writing operation of a representation of the pixel in a memory cell of the frame buffer identified by the virtual address.

10 ~~15.~~ The method of claim ~~14,~~ 9 further comprising:

f) repeating c) through e) for each of a plurality of pixels of the display panel.

16. The method of claim 14, further comprising:

f) defining a base value, and wherein the first dimension of the virtual frame buffer is a power of the base value.

17. The method of claim 16, wherein the first and second coordinates of the pixel are stored as bit representations and the base value is defined as a power of two.

18. The method of claim 14, wherein the first and second coordinates of the pixel are stored as bit representations and d) comprises:

f) removing a quantity of bits from the bit representation of the second coordinate of the pixel equal in number to the length of the second tile span and concatenating the quantity bits with the bits of the bit representation of the first coordinate of the pixel; and

g) concatenating with the result of f) bits of the bit representation of the second coordinate of the pixel less the quantity of bits.

19. The method of claim 14, wherein d) comprises converting the generated virtual address into a frame buffer address in a frame buffer address range of the frame buffer and performing one of a reading operation and a writing operation of a representation of the pixel in a memory cell of the frame buffer identified by the frame buffer address.

20. The method of claim 14, wherein d) comprises performing one of a reading operation and a writing operation of a representation of the pixel in a memory cell identified by the virtual address in a frame buffer addressed by virtual

addresses.

15 21. The method of claim 20, wherein the frame buffer is addressed by the addresses of the virtual frame buffer that represent virtual addresses of pixels of the display panel.

SUB B2 22. A system for remapping between pixel coordinate space and memory address space, comprising:

a central processing unit;

a frame buffer memory coupled to the central processing unit and having an associated memory address scheme;

a memory address device coupled to the central processing unit for defining a phantom port containing a plurality of memory addresses, each of a subset of the memory addresses mapping to an address in the frame buffer memory; and

a remapping device coupled to the memory address device for converting an address between the memory address scheme of the frame buffer memory and a memory address of the phantom port.

23. The system of claim 22, wherein the defined phantom port has a span equal in size to a power of two, and wherein the remapping device comprises at least one field extractor for extracting fields from the memory address of the phantom port.

24. A system for accessing representations of pixels for a display panel in a frame buffer, each pixel having a first coordinate and a second coordinate, comprising:

a processing unit;

a data accessing module for converting pixel coordinates to virtual frame buffer addresses;

a video controller for transmitting video data;

a system memory including a frame buffer for storing digital video data;

a bus coupled to the processing unit, the data accessing module, the video controller, and the system memory, for transmitting data therebetween; and

a display system coupled to the video controller for receiving and displaying video data on the display panel.

25. The system of claim 24, wherein the system memory further comprises an address decoder for decoding read and write requests and further for determining a memory location within the frame buffer.

26. The system of claim 24, wherein the virtual frame buffer addresses are arranged to form a virtual frame buffer having a span equal to a power of two, and wherein the data accessing module converts pixel coordinates to virtual frame buffer addresses using concatenation.

27. The system of claim 26, wherein the first and second coordinates of the pixel are stored as bit representations and wherein the data accessing module converts pixel coordinates to virtual frame buffer addresses by concatenating the bit representation of the first coordinate of the pixel to the bit representation of the second coordinate of the pixel.

28. The system of claim 24, wherein the data accessing module further converts virtual frame buffer addresses to pixel coordinates.

29. The system of claim 28, wherein the virtual frame buffer addresses are ar-

ranged to form a virtual frame buffer having a span equal to a power of two, and wherein the data accessing module converts virtual frame buffer addresses to pixel coordinates using bit field extraction.